BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/031,326	02/26/1998	JOSEPH J. KARNIEWICZ	303.376US1	8474

21186 7590 08/04/2004

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
PHAN, THAI Q	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 08/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/031,326	KARNIEWICZ, JOSEPH J.
	Examiner	Art Unit
	Thai Q. Phan	2128

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 8/4/00 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *Jan. 31, 2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to applicant's amendment filed 05/03/2004. Claims 1-36 are pending in this Action.

Specification

The attempt to incorporate subject matter into this application by reference to a co-pending and co-assigned as disclosed in the present application is incomplete because it does not provide current status and complete US patent application Serial Number of the co-pending and co-assigned to make the record clear and complete. Applicant is requested to provide a current status of the co-pending and co-assigned application as disclosed in the present application.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on Jan. 9, 2001 was considered. A copy of the IDS is enclosed in this Office Action as requested by the applicant.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Madhavan et al, US patent no. 5,675,545 in views of Ho, William, US patent no. 6,421,814 B1 ('814) and Ho et al, US patent no. 6,009,251 ('251).

As per claims 1 and 9, Madhavan discloses an integrated circuit design and design methodology employing cell hierarchical structure with feature limitations substantially similar to the claimed invention (col. 2, lines 2-25, for exemplary). According to Madhavan, the design apparatus for integrated circuit design includes physical design files representing for integrated design cells including global variables and design data relating to layout or schematics layout and connectivity data of the functional block, a plurality of cell configuration files or claimed local files, each relating a plurality of local variables to the global variables in system files (Figs. 9, 10-11, col. 2, lines 27-44, col. 5, line 50 to col. 6, line 47, col. 8, lines 31-50, for example), and a plurality of cells, each cell corresponding to a local file and having a set of parameters derived by relating the local variables to the global variables in the global source files such that the changes of global variables in the global files reflect or may cause changes in the programmable cells, including layout of the hierarchical semiconductor structure in accordance with parameters in the local files (Figs. 5-10, col. 6, line 48 to col. 8, line 50).

The physical semiconductor memory with memory cells in Madhavan integrated chip design occupied a physical area on the semiconductor substrate, and the physical design area takes geometric shape or size having geometric parameter values for physical cell placement in an hierarchical manner, such as relationships between cells,

cell size, between-cell interconnections, etc, on the semiconductor substrate. Madhavan does not expressly disclose geometric variables in design file relationships as claimed.

Such geometrical variables and feature relationships in the design hierarchical manner as claimed is well-known in the semiconductor circuit design, and layout and placement. In fact, Ho ('814) teaches geometrical layout variables or parameters and relationships of geometrical variables in geometrical layout data files in physical design for improving layout control mechanism (Background of the Invention, col. 1, lines 48-60, Fig. 1B, col. 5, lines 33-60, col. 8, lines 9-21, col. 9, lines 17-24, for example). Ho ('251) also teaches an improved method and system for physical cell design by incorporating local geometry and parent references such as global geometrical variables, local variables, and global and local variable relationships for hierarchical cell layout design and cell interconnection verification (Figs. 2-4, col. 3, lines 25-67, col. 7, lines 7-36, col. 8, line 29 to col. 10, line 43, for example) in order to reduce cell layout design cycle and verification time as taught in Ho. By using geometrical relations between global variables and local variables in design files, a large number of physical design files in Madhavan design process (col. 6, lines 40-43, for instance) would be simplified and the design time would be saved as taught in Ho ('251) (col. 2, lines 60-63, col. 3, lines 43-50).

This would motivate practitioner in the art at the time of the invention was made to use Ho teachings of geometrical layout variables in hierarchical relationships for physical design of the integrated circuit as disclosed in Madhavan to improve layout

processing time and speed up design process, design verification and circuit testing as in Madhavan.

As per claims 2-3 and 10-11, Madhavan discloses local files would obviously include inherent file from source files, instance files, data files, etc. (Figs. 9-11).

As per claim 4, Madhavan discloses master files in hierarchical design acting as initial version of a corresponding local file for design, modification, increment compilation, etc.

As per claim 5, Madhavan discloses file or clean sheet file for containing design rules for a plurality of cells for coordinated design as claimed.

As per claim 6, Madhavan discloses file extraction and related variable extraction for design and update design.

As per claims 7-8, Madhavan discloses the design display in local host for display interactively interface.

As per claim 12, Madhavan discloses file update including update global file for coordinate process.

As per claim 13, Madhavan discloses local display in local user workstation for the design process.

As per claim 14, Madhavan discloses computer program in concurrent with design program for circuit design process as claimed.

As per claim 15, Madhavan discloses a method and design system for designing and testing semiconductor memory with feature limitations substantially similar to the claimed invention (Abstract and "Summary of the Invention"). According to Madhavan,

the design apparatus includes global files for global variables and design data relating to layout or schematics layout and connectivity data of the functional block, a plurality of cell configuration files or claimed local files, each relating a plurality of local variables to the global variables in system files (Figs. 9, 10-11, col. 2, lines 27-44, col. 5, line 50 to col. 6, line 47, col. 8, lines 31-50, for example), and a plurality of cells, each cell corresponding to a local file and having a set of parameters derived by relating the local variables to the global variables in the global source files such that the changes of global variables in the global files reflect or may cause changes in the programmable cells, including layout of the hierarchical semiconductor structure in accordance with parameters in the local files (Figs. 5-10, col. 6, line 48 to col. 8, line 50). Madhavan does not expressly disclose geometric variables related to physical layout in hierarchical manner as claimed.

Physical semiconductor memory with memory cells in Madhavan integrated chip design occupied a physical area on the semiconductor substrate, and the physical design area usually takes geometric shape or sizes taking geometric parameter values for hierarchical cell placement on the semiconductor substrate

Madhavan does not expressly disclose geometric variables in design file relationships for the design process as claimed.

Such geometrical variables and feature relationships in the design hierarchical manner as claimed is well-known in the semiconductor circuit design, and layout and placement. In fact, Ho ('814) teaches geometrical layout variables or parameters and relations of geometrical variables in geometrical layout data file to improve layout

control mechanism for physical design (Background of the Invention, col. 1, lines 48-60, Fig. 1B, col. 5, lines 33-60, col. 8, lines 9-21, for example). Ho ('251) also teaches an improved method and system for physical cell design by incorporating local geometry and parent references such as global geometrical variables, local variables, and global and local variable relationships for hierarchical cell layout design and cell interconnection verification (Figs. 2-4, col. 3, lines 25-67, col. 7, lines 7-36, col. 8, line 29 to col. 10, line 43, for example) in order to reduce cell layout design cycle and verification time as taught in Ho. By using geometrical relations between global variables and local variables in design files, a large number of physical design files in Madhavan design process (col. 6, lines 40-43, for instance) would be simplified and the design time would be saved as taught in Ho ('251) (col. 2, lines 60-63, col. 3, lines 43-50).

By using geometrical relations between global variables and local variables in design files, a large number of physical design files in Madhavan design process (col. 6, lines 40-43, for instance) would be simplified and the design time was saved as taught in Ho ('251) (col. 2, lines 60-63, col. 3, lines 43-50).

This would motivate practitioner in the art at the time of the invention was made to use Ho teachings of geometrical layout variables in hierarchical relationships for physical design of the integrated circuit as disclosed in Madhavan to improve layout processing time and speed up design process, design verification and circuit testing as in Madhavan.

As per claims 16-21, similarly, with the rejection rationale above, the claims are also rejected due to its similarities to claims 2-8 and claims 11-14.

As per claim 22, Madhavan discloses a method and design system for designing and testing semiconductor memory with feature limitations substantially similar to the claimed invention (Abstract and "Summary of the Invention"). According to Madhavan, the design apparatus includes

A processor (Figs. 8 and 9),

A computer readable medium (Figs. 8 and 9, col. 6, lines 35-47),

global files for global variables and design data relating to layout or schematics layout and connectivity data of the functional block, a plurality of cell configuration files or claimed local files, each relating a plurality of local variables to the global variables in system files (Figs. 9, 10-11, col. 2, lines 27-44, col. 5, line 50 to col. 6, line 47, col. 8, lines 31-50, for example), and a plurality of cells, each cell corresponding to a local file and having a set of parameters derived by relating the local variables to the global variables in the global source files such that the changes of global variables in the global files reflect or may cause changes in the programmable cells, including layout of the hierarchical semiconductor structure in accordance with parameters in the local files (Figs. 5-10, col. 6, line 48 to col. 8, line 50).

Physical semiconductor memory with memory cells in Madhavan integrated chip design occupied a physical area on the semiconductor substrate, and the physical design area has geometric shape or sizes taking geometric parameter values for hierarchical placement of cells on the semiconductor substrate. Madhavan does not

expressly disclose geometric variables in files relationships for physical layout design in an hierarchical manner as claimed.

Such geometrical variables and feature relationships in the design hierarchical manner as claimed is well-known in the semiconductor circuit design, and layout and placement. In fact, Ho ('814) teaches geometrical layout variables or parameters and relations of geometrical variables in geometrical layout data for physical design with faster and better layout mechanism in integrated circuit design (Background of the Invention, col. 1, lines 48-60, Fig. 1B, col. 5, lines 33-60, cols. 8, 9, for example). Ho ('251) also teaches an improved method and system for physical cell design by incorporating local geometry and parent references such as global geometrical variables, local variables, and global and local variable relationships for hierarchical cell layout design and cell interconnection verification (Figs. 2-4, col. 3, lines 25-67, col. 7, lines 7-36, col. 8, line 29 to col. 10, line 43, for example) in order to reduce cell layout design cycle and verification time as taught in Ho. By using geometrical relations between global variables and local variables in design files, a large number of physical design files in Madhavan design process (col. 6, lines 40-43, for instance) would be simplified and the design time would be saved as taught in Ho ('251) (col. 2, lines 60-63, col. 3, lines 43-50).

This would motivate practitioner in the art at the time of the invention was made to use Ho teachings of geometrical layout variables in hierarchical relationships for physical design of the integrated circuit as disclosed in Madhavan to improve layout

processing time and speed up design process, design verification and circuit testing as in Madhavan.

As per claims 23-24, Madhavan and Ho disclose inherent design file, and instance file in the design database.

As per claim 25, Ho ('251) disclosure would imply design framework for use in the chip design process. Such design framework would include not limited to CADENCE functional design system as claimed.

As per claims 26, 30, and 33, Madhavan discloses a method and design system for designing and testing semiconductor memory with feature limitations substantially similar to the claimed invention (Abstract and "Summary of the Invention"). According to Madhavan, the design apparatus includes global files for global variables and design data relating to layout or schematics layout and connectivity data of the functional block, a plurality of cell configuration files or claimed local files, each relating a plurality of local variables to the global variables in system files (Figs. 9, 10-11, col. 2, lines 27-44, col. 5, line 50 to col. 6, line 47, col. 8, lines 31-50, for example), and a plurality of programmable cells (Background of the Invention), each cell corresponding to a local file and having a set of parameters derived by relating the local variables to the global variables in the global source files such that the changes of global variables in the global files reflect or may cause changes in the programmable cells, including layout of the hierarchical semiconductor structure in accordance with parameters in the local files (Figs. 5-10, col. 6, line 48 to col. 8, line 50).

Physical semiconductor memory with memory cells in Madhavan integrated chip design occupied a physical area on the semiconductor substrate, and the physical design area has geometric shape or sizes taking geometric parameter values for hierarchical placement of cells on the semiconductor substrate. Madhavan does not expressly disclose geometric variables related to physical layout in a hierarchical manner as claimed.

Such geometrical variables and feature relationships in the design hierarchical manner as claimed is well-known in the semiconductor circuit design, and layout and placement. In fact, Ho ('814) teaches geometrical layout variables or parameters and relations of geometrical variables in geometrical layout data for physical design with faster and better layout mechanism in integrated circuit design (Background of the Invention, col. 1, lines 48-60, Fig. 1B, col. 5, lines 33-60). Ho ('251) also teaches an improved method and system for physical cell design by incorporating local geometry and parent references such as global geometrical variables, local variables, and global and local variable relationships for hierarchical cell layout design and cell interconnection verification (Figs. 2-4, col. 3, lines 25-67, col. 7, lines 7-36, col. 8, line 29 to col. 10, line 43, for example) in order to reduce cell layout design cycle and verification time as taught in Ho. By using geometrical relations between global variables and local variables in design files, a large number of physical design files in Madhavan design process (col. 6, lines 40-43, for instance) would be simplified and the design time would be saved as taught in Ho ('251) (col. 2, lines 60-63, col. 3, lines 43-50).

By using geometrical relations between global variables and local variables in design files, a large number of physical design files in Madhavan design process (col. 6, lines 40-43, for instance) was simplified and the design time would be saved as taught in Ho ('251) (col. 2, lines 60-63, col. 3, lines 43-50).

This would motivate practitioner in the art at the time of the invention was made to use Ho teachings of geometrical layout variables in hierarchical relationships for physical design of the integrated circuit as disclosed in Madhavan to improve layout processing time and speed up design process, design verification and circuit testing as in Madhavan.

As per claims 27 and 28, Madhavan discloses global files and related parameters files in the semiconductor memory design. Such design parameter files could include inherent files and instance files as claimed.

As per claim 29, Madhavan and Ho disclose means for displaying design process.

As per claim 31, Madhavan discloses update design data in database spreadsheet such as in cleansheet file (col. 7, lines 1-5, for example).

As per claim 32, Madhavan discloses the display means for value changes, design files, and means for allowance of user interface.

As per claims 34-36, Ho ('251) disclosure the claimed limitations in the parametric design process.

Response to Arguments

3. In response to applicant's argument that there is no suggestion to combine the references to produce the claimed invention for non-related references and lack of motivation, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the subject matters in the references are related to each other. They are related to physical functional circuit design well-known in the art. They are directed to methods and systems for physical circuit design and layout placement design to improve design and verification process (see Madhavan, col. 2, lines 2-5, lines 35-48, col. 6, lines 35-45, for illustration of integrated cells physical design in an hierarchical manner). It's clear Madhavan disclosure is dealt with physical cell design and placement, particularly for memory cells design and verification.

4. Ho ('251) also teaches an improved method for integrated physical cells design by implementing physical cells with geometrical variables in global and local subcell design with local/global geometrical variable relationships for hierarchical cell layout design and cell interconnection verification (Figs. 2-4, col. 3, lines 25-67, col. 7, lines 7-36, col. 8, line 29 to col. 10, line 43, for example) in order to reduce cell layout design cycle and verification time. It's because by using geometrical relationhips between

global variables and local variables in design files, a large number of physical design files in Madhavan physical design process (col. 6, lines 40-43, for instance) would be simplified and the design time was saved as taught in Ho ('251) (col. 2, lines 60-63, col. 3, lines 43-50).

This would motivate practitioner in the art at the time of the invention was made to use Ho ('251 and '814) teachings of geometrical layout variables in hierarchical relationships for physical design of the integrated circuit as disclosed in Madhavan to improve layout processing time and speed up physical design process and design verification for a large scale integrated circuit of Madhavan.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Q. Phan whose telephone number is 703-305-3812. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703-305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

7. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

July 20, 2004

Thai Phan
Patent Examiner
Art Unit 2128